REMARKS

Claims 1-20 remain in the present application. Claims 1, 3, 6-7, 10, 13, 17 and 19 are amended herein. Applicants respectfully submit that no new matter has been added as a result of the claim amendments. Applicants respectfully request further examination and reconsideration of the rejections based on the arguments set forth below.

Claim Rejections – 35 U.S.C. §112

Claims 1-16 are rejected under 35 U.S.C. §112, first paragraph, for allegedly failing to comply with the written description requirement. More specifically, page 2 of the rejection states that the combination of elements of "a reference signal that is inversely proportional to said temperature" as recited in independent Claims 1 and 10 and the combination of elements of "wherein components of said second circuit are placed in a fixed state during manufacturing" as recited in Claim 3 are allegedly not supported by the specification as filed. Independent Claims 1 and 10 are amended herein to recite the combination of elements of "wherein said delay is inversely proportional to said temperature" which are supported, for example, by lines 9-10 of page 18 of the instant specification. Additionally, Claim 3 is amended herein to recite the combination of elements of "wherein said plurality of individually-configured components of said first circuit are placed in a fixed state during manufacturing" which are supported, for example, by Figure 3 and line 22 of page 10 to line 10 of page 11 of the instant specification. Accordingly, Applicants respectfully submit

that Claims 1-16 comply with 35 U.S.C. §112, first paragraph, in light of the claim amendments made herein.

Claim Rejections – 35 U.S.C. §103

Claims 1-20 are rejected under 35 U.S.C. §103(a) as being allegedly unpatentable over United States Patent Number 5,994,937 to Hara et al. (referred to herein as "Hara"), in view of United States Patent Number 5,926,045 to Kwon (referred to herein as "Kwon"), further in view of United States Patent Number 6,031,366 to Mitsuishi (referred to herein as "Mitsuishi"), and further in view of United States Patent Number 6,388,490 to Saeki (referred to herein as "Saeki"). Applicants respectfully submit that the embodiments as recited in Claims 1-20 are not rendered obvious by Hara in view of Kwon, further in view of Mitsuishi, and further in view of Saeki for the following reasons.

Applicants respectfully direct the Examiner to independent Claim 1, which recites a timer circuit comprising:

> an output stage coupled to a configurable delay element, wherein said configurable delay element comprises a plurality of selectively-activated components operable to adjust a delay through said timer circuit; and
>
> a pull-down path coupled to said output stage and comprising a first circuit for providing a selectable amount of pull down current, wherein said first circuit comprises a plurality of individually-configured components, wherein said plurality of selectively-activated components are of a different component type than said plurality of individually-configured components, said pull-down path further comprising a second circuit for varying said delay through said timer circuit based upon temperature, wherein said second circuit is operable to vary said delay based upon a reference signal, and wherein said delay is inversely proportional to said temperature.

Claims 2-9 depend from independent Claim 1 and recite further elements of the claimed invention.

Applicants respectfully direct the Examiner to independent Claim 10, which recites an electronic device comprising a timer circuit, wherein the timer circuit comprises:

> an output stage coupled to a configurable delay element, wherein said configurable delay element comprises a plurality of selectively-activated components operable to adjust a delay through said timer circuit; and
>
> a pull-down path coupled to said output stage and comprising a first circuit for providing a selectable amount of pull down current, wherein said first circuit comprises a plurality of individually-configured components, wherein said plurality of selectively-activated components are of a different component type than said plurality of individually-configured components, said pull-down path further comprising a second circuit for varying said delay through said timer circuit based upon temperature, wherein said second circuit is operable to vary said delay based upon a reference signal, wherein said delay is inversely proportional to said temperature, and wherein said reference signal is derived from a band gap reference circuit.

Claims 11-16 depend from independent Claim 10 and recite further elements of the claimed invention.

Applicants respectfully direct the Examiner to independent Claim 17, which recites a method of varying a delay of a timer circuit comprising (emphasis added):

> during configuration of said timer circuit, setting a first plurality of configuration bits which control the amount of elements coupled to an output stage of said timer circuit to set an amount of delay through said timer circuit;
>
> during said configuration, setting a second plurality of configuration bits which control an amount of pull down current through a pull down path of said timer circuit to set an amount of delay through said timer circuit, said pull down path coupled to said output stage, wherein said pull down

path comprises a plurality of individually-configured components, and wherein each of said plurality of individually-configured components corresponds to a respective configuration bit of said plurality of configuration bits; and

during operation of said timer circuit, varying said delay of said timer circuit in response to a varying of a reference signal, wherein said delay of said timer circuit is inversely proportional to a temperature of said timer circuit.

Claims 18-20 depend from independent Claim 17 and recite further elements of the claimed invention.

Applicants respectfully submit that Hara, Kwon, Mitsuishi and/or Saeki, either alone or in combination, fail to teach or suggest the elements of "a pull-down path... comprising a first circuit for providing a selectable amount of pull down current, wherein said first circuit comprises a plurality of individually-configured components" as recited in independent Claims 1 and 10 and the elements of "wherein said pull down path comprises a plurality of individually-configured components, and wherein each of said plurality of individually-configured components corresponds to a respective configuration bit of said plurality of configuration bits" as recited in independent Claim 17. As recited and described in the present application, a pull-down path includes a first circuit for providing a selectable amount of pull down current. The first circuit comprises a plurality of individually-configured components (e.g., transistors 344, 348, 352 and 356 of Figure 3). In one embodiment, each of the plurality of individually-configured components may correspond to a respective configuration bit of a plurality of configuration bits (e.g., configuration bits corresponding to signals tm1-tm4 323a-323d of Figure 3).

In contrast to the claimed embodiments, Applicants understand the cited Hara/Kwon/Mitsuishi/Saeki combination to teach a current mirror (e.g., current mirror 20 as taught by Figure 2 of Kwon) which receives a single signal from a current source (e.g., current source IS1 as taught by Figure 2 of Kwon). Assuming arguendo that components of Kwon's current mirror 20 are analogous to the claimed plurality of individually-configurable components, Applicants respectfully submit that the cited Hara/Kwon/Mitsuishi/Saeki combination teaches away from the claimed embodiments by teaching that the components of current mirror 20 are configured by a *single* signal from current source IS1 and therefore are not individually configured (e.g., each receiving a respective configuration signal) as claimed.

Applicants respectfully submit that Hara, Kwon, Mitsuishi and/or Saeki, either alone or in combination, fail to teach or suggest the limitations of "wherein said individually-configured components of said first circuit are placed in a fixed state during manufacturing" as recited in Claim 3. As recited and described in the present application, the individually-configured components of the first circuit are placed in a fixed state during manufacturing. For example, the components of the first circuit may be fusible links, metal options, bond options, etc.

In contrast to the claimed embodiments, Applicants respectfully submit that the cited Hara/Kwon/Mitsuishi/Saeki combination fails to teach or suggest components placed in a fixed state during manufacturing as claimed. More specifically, Kwon fails to teach or suggest that current source IS1 comprises a

plurality of individually-configured components which are placed in a fixed state during manufacturing as claimed. Accordingly, Applicants reiterate that Hara, Kwon, Mitsuishi and/or Saeki, either alone or in combination, fail to teach or suggest the limitations of "wherein said individually-configured components of said first circuit are placed in a fixed state during manufacturing" as recited in Claim 3.

For these reasons, Applicants respectfully submit that independent Claims 1, 10 and 17 are not rendered obvious by Hara in view of Kwon, further in view of Mitsuishi, and further in view of Saeki, thereby overcoming the 35 U.S.C. §103(a) rejections of record. Since Claims 2-9, 11-16 and 18-20 recite further elements of the invention claimed in their respective independent claims, Claims 2-9, 11-16 and 18-20 also overcome the 35 U.S.C. §103(a) rejections of record. Therefore, Claims 1-20 are allowable.

CONCLUSION

Applicants respectfully submit that Claims 1-20 are in condition for allowance and Applicants earnestly solicit such action from the Examiner.

The Examiner is urged to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Please charge any additional fees or apply any credits to our PTO deposit account number: 50-4160.

Respectfully submitted,

MURABITO, HAO & BARNES LLP

Dated: 1 / 21 / 2009 /BMF/

Bryan M. Failing
Registration No. 57,974

Two North Market Street
Third Floor
San Jose, CA 95113
(408) 938-9060